UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,175	04/06/2001	Michael Sokol	023925-00003	4372

32294 7590 08/02/2005

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
YAO, KWANG BIN	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,175	SOKOL ET AL.	
	Examiner	Art Unit	
	Kwang B. Yao	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-15* is/are rejected.

7)☒ Claim(s) *2 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/18/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Erimli et al. (US 6,760, 341).

Erimli et al. discloses a communication system comprising the following features: regarding claim 13, a method for sharing memory between a first switch (Fig. 2, switch 22a) and a second switch (Fig. 2, switch 22b) connected to each other by an expansion bus (Fig. 2, bus 32) comprising the steps of: sending a command from a first switch (Fig. 2, switch 22a) to a second switch (Fig. 2, switch 22b) that said first switch (Fig. 2, switch 22a) is about to perform a

memory read or write (column 5, lines 15-19); reading or writing (column 5, lines 15-19) a portion of packet data to local memory of said first switch (Fig. 2, switch 22a) using a memory bus (Fig. 2, bus 38); and reading or writing (column 5, lines 15-19) another portion of packet data to alternate memory through said second switch (Fig. 2, switch 22b) using said expansion bus (Fig. 2, bus 32). See column 1-6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-9, 11, 12, 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erimli et al. (US 6,760, 341) in view of Smith (US 6,011,793).

Erimli et al. discloses a communication system comprising the following features: regarding claim 1, a first switch (Fig. 2, switch 22a) having a first memory (Fig. 2, memory 36a), interface and a first expansion port (Fig. 2, expansion port 30); a first memory (Fig. 2, memory 36a) coupled to the first switch (Fig. 2, switch 22a) with a first memory (Fig. 2, memory 36a) bus (Fig. 2, bus 38); an expansion bus (Fig. 2, bus 32) having a first expansion bus (Fig. 2, bus 32) interface and a second expansion bus (Fig. 2, bus 32) interface, said first expansion bus (Fig. 2, bus 32) interface connected to said first expansion port (Fig. 2, expansion port 30); and a second switch (Fig. 2, switch 22b) having a second memory interface (Fig. 2, memory 44b) and a second expansion port (Fig. 2, expansion port 30), said second expansion port (Fig. 2, expansion

port 30) connected to said second expansion bus (Fig. 2, bus 32) interface, thereby connecting said first switch (Fig. 2, switch 22a) to said second switch (Fig. 2, switch 22b); and a second memory (Fig. 2, memory 36b) coupled to the second switch (Fig. 2, switch 22b) with a second memory (Fig. 2, memory 36b) bus (Fig. 2, bus 38); regarding claim 3, wherein said first memory interface (Fig. 2, memory 44a) is configured to be connected to the first external memory and said second memory interface (Fig. 2, memory 44b) is configured to be connected to the second memory (Fig. 2, memory 36b); regarding claim 4, a command bus (column 6, lines 9-15) connected between said first switch (Fig. 2, switch 22a) and said second switch (Fig. 2, switch 22b) allowing commands to be communicated between said first switch (Fig. 2, switch 22a) and said second switch (Fig. 2, switch 22b); regarding claim 5, a memory interface that accesses memory via a memory bus (Fig. 2, bus 38); and an expansion port (Fig. 2, expansion port 30) connected to said memory interface; regarding claim 6, wherein said expansion port (Fig. 2, expansion port 30) further comprises a proxy (Fig. 2, switching logic 28) component that when activated allows data packets to be written (column 5, lines 15-19) to said memory from another switch through said expansion port (Fig. 2, expansion port 30); regarding claim 7, wherein said memory interface is configured to access external memory; regarding claim 8, a command bus (column 6, lines 9-15) interface configured to be connected to another switch allowing commands to be communicated between switches; regarding claim 9, a first switch (Fig. 2, switch 22a) having a first memory (Fig. 2, memory 36a) and a first expansion port (Fig. 2, expansion port 30); an expansion bus (Fig. 2, bus 32) having a first expansion bus (Fig. 2, bus 32) end and a second expansion bus (Fig. 2, bus 32) end, said first expansion bus (Fig. 2, bus 32) end connected to said first expansion port (Fig. 2, expansion port 30); and a second switch (Fig.

2, switch 22b) having a second memory (Fig. 2, memory 36b) and a second expansion port (Fig. 2, expansion port 30), said second expansion port (Fig. 2, expansion port 30) connected to said second expansion bus (Fig. 2, bus 32) end, thereby connecting said first switch (Fig. 2, switch 22a) to said second switch (Fig. 2, switch 22b); regarding claim 11, wherein said first memory (Fig. 2, memory 36a) is external memory and said second memory (Fig. 2, memory 36b) is external memory; regarding claim 12, a command bus (column 6, lines 9-15) connected between said first switch (Fig. 2, switch 22a) and said second switch (Fig. 2, switch 22b) allowing commands to be communicated between said first switch (Fig. 2, switch 22a) and said second switch (Fig. 2, switch 22b); regarding claim 14, wherein said step of sending a command further comprises configuring said second switch (Fig. 2, switch 22b) to be a proxy (Fig. 2, switching logic 28) allowing said packet data to written (column 5, lines 15-19) to said second memory (Fig. 2, memory 36b) by said first switch (Fig. 2, switch 22a) through said expansion bus (Fig. 2, bus 32); regarding claim15, wherein said step of sending a command comprises the step of sending said command across a command bus (column 6, lines 9-15) connected between said first switch (Fig. 2, switch 22a) and said second switch (Fig. 2, switch 22b) allowing commands to be communicated between said first switch (Fig. 2, switch 22a) anal said second switch (Fig. 2, switch 22b). See column 1-6.

Erimli et al. does not disclose the following features: regarding claim 1, wherein said expansion bus allows said first switch to directly access said second memory interface through said second switch and said second switch to directly access said first memory interface through said first switch to increase a bandwidth of a read/write operation to the first memory and the second memory; regarding claim 5, wherein said expansion port is configured to be connected to

an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read/write operation; regarding claim 6, wherein said expansion port further comprises a proxy component that when activated allows data packets to be read from said memory from another switch through said expansion port; regarding claim.9, wherein said expansion bus allows said first switch to directly access said second memory through said second switch and said second switch to directly access said first memory through said first switch to increase a bandwidth of a read/write operation to the first memory and the second memory; regarding claim 14, wherein said step of sending a command further comprises configuring said second switch to be a proxy allowing said packet data to be read from said second memory by said first switch through said expansion bus.

Smith discloses a communication system comprising the following features: regarding claim 1, wherein said expansion bus allows said first switch (Fig. 3, switch 200) to directly access said second memory (Fig. 3, memory 241) interface through said second switch (Fig. 3, switch 201) and said second switch (Fig. 3, switch 201) to directly access said first memory (Fig. 3, memory 240) interface through said first switch (Fig. 3, switch 200) to increase a bandwidth of a read (column 6, lines 43-65)/write operation to the first memory (Fig. 3, memory 240) and the second memory (Fig. 3, memory 241) ; regarding claim 5, wherein said expansion port is configured to be connected to an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read (column 6, lines 43-65)/write operation; regarding claim 6, wherein said expansion port further comprises a proxy component that when activated allows data packets to be read (column 6, lines 43-65) from said memory from another switch through said expansion port; regarding

claim 9, wherein said expansion bus allows said first switch (Fig. 3, switch 200) to directly access said second memory (Fig. 3, memory 241) through said second switch (Fig. 3, switch 201) and said second switch (Fig. 3, switch 201) to directly access said first memory (Fig. 3, memory 240) through said first switch (Fig. 3, switch 200) to increase a bandwidth of a read (column 6, lines 43-65)/write operation to the first memory (Fig. 3, memory 240) and the second memory (Fig. 3, memory 241) ; regarding claim 14, wherein said step of sending a command further comprises configuring said second switch (Fig. 3, switch 201) to be a proxy allowing said packet data to be read (column 6, lines 43-65) from said second memory (Fig. 3, memory 241) by said first switch (Fig. 3, switch 200) through said expansion bus. See column 1-13. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Erimli et al., by using the features, as taught by Smith, in order to provide an efficient system by activating the appropriate bus line units in turn over the course of the reading phase to facilitate data transfer from the memory means to the switch unit of each selected pair for the switch unit concerned. See Smith, column 5, lines 12-15.

Allowable Subject Matter

6. Claims 2 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sang et al. (US 6,741,589) discloses multiple network switch modules.

Sang (US 6,724,769) discloses multiple network switch modules.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 571-272-3182. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

Kwang B. Yao
August 1, 2005